IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 3 and 35-51, AMEND claims 1, 2, 21 and 24 and add new claims 52-55 in accordance with the following:

1. (currently amended) A multi-layer circuit wiring board comprising a laminate of films and an adhesive layer for bonding said films, each film having a wiring pattern formed on at least one surface thereof, wherein the wiring pattern formed on each film is electrically connected with the wiring pattern formed on another film which is disposed neighboring thereto through a via-contact layer formed in any one of the neighboring films, each of said films having a thickness of 12.5 μm to 80 μm, and said adhesive layer having a thickness of 30 μm or less.

2. (original) The multi-layer circuit wiring board according to claim 1, wherein all of said films have almost the same thickness.

3. (cancelled)

4. (withdrawn) A multi-layer circuit wiring board comprising:

a first film having a first wiring pattern formed on one surface thereof, a second wiring pattern formed on another surface thereof, and a first via-contact layer electrically connecting said first wiring pattern with said second wiring pattern;

a second film provided with a third wiring pattern for mounting an IC on one surface thereof, another surface thereof being superimposed on said one surface of said first film;

a third film provided on one surface thereof with a fourth wiring pattern to be electrically connected with a printed wiring board, another surface thereof being superimposed on the other surface of said first film;

a second via-contact layer for electrically connecting said first wiring pattern with said third wiring pattern; and

a third via-contact layer for electrically connecting said second wiring pattern with said fourth wiring pattern.

5. (withdrawn) The multi-layer circuit wiring board according to claim 4, wherein said first film comprises a polyimide resin layer, and a first and a second wiring patterns each formed of copper and formed on said polyimide resin layer; said second film comprises a polyimide resin layer and a third wiring pattern formed of copper and formed on said polyimide resin layer; and said third film comprises a polyimide resin layer and a fourth wiring pattern formed of copper and formed on said polyimide resin layer.

6. (withdrawn) The multi-layer circuit wiring board according to claim 5, wherein a surface roughness of that surface of the polyimide resin layer on which said wiring pattern is formed, is within a range of 0.01 μm to 5.0 μm based on an average roughness as measured at optional ten points, said polyimide resin layer being at least one film selected from the group consisting of said first film, second film and third film.

7. (withdrawn) The multi-layer circuit wiring board according to claim 5, wherein a line width of said wiring pattern formed on said polyimide resin layer is 50 m or less, said polyimide resin layer being at least one film selected from the group consisting of said first film, second film and third film, and a surface roughness of said polyimide resin layer is within a range of 0.01 μm to 5.0 μm based on an average roughness as measured at optional ten points.

8. (withdrawn) The multi-layer circuit wiring board according to claim 5, which further comprises a first adhesive layer for bonding said second film to said first film, and a second adhesive layer for bonding said third film to said first film.

9. (withdrawn) The multi-layer circuit wiring board according to claim 8, wherein said adhesive layers are formed of a thermosetting adhesive layer containing an epoxy curing component.

10. (withdrawn) The multi-layer circuit wiring board according to claim 8, wherein a thickness of each of said adhesive layers is 301 μm or less.

11. (withdrawn) The multi-layer circuit wiring board according to claim 4, wherein said first via-contact layer, second via-contact layer and third via-contact layer are formed of a blind via-contact layer, and a ratio of diameter of a bottom of each of these via-contact layers to diameter of a top opening of each of these via-contact layers is within a range of 0.2 to 1.0.

12. (withdrawn) The multi-layer circuit wiring board according to claim 4, wherein said first via-contact layer, second via-contact layer and third via-contact layer are formed of a blind via-contact layer, and a ratio of diameter of a bottom of each of these via-contact layers to diameter of a top opening of each of these via-contact layers is within a range of 0.4 to 0.8.

13. (withdrawn) The multi-layer circuit wiring board according to claim 4, wherein value of (value of a top opening of each of these via-contact layers)/(total value of a thickness of the conductor layer+a thickness of the second film or the third film+a thickness of the first adhesive layer or of the second adhesive layer) or value of (value of a top opening of each of these via-contact layers)/(total value of a thickness of the conductor layer+a thickness of the first film) is 1.5 or less.

14. (withdrawn) A multi-layer circuit wiring board comprising:

a first film having a first wiring pattern formed on one surface thereof; and

a second film provided with a third wiring pattern for mounting an IC on one surface thereof, another surface thereof being superimposed on said one surface of said first film;

wherein said second film is provided with a first via-contact layer for electrically connecting said first wiring pattern with said third wiring pattern.

15. (withdrawn) The multi-layer circuit wiring board according to claim 14, wherein said first film comprises a polyimide resin layer and a first wiring pattern formed of copper and formed on said polyimide resin layer; and

said second film comprises a polyimide resin layer and a third wiring pattern formed of copper and formed on one surface of said polyimide resin layer.

16. (withdrawn) The multi-layer circuit wiring board according to claim 14, which further comprises a fixing frame which is attached by means of an adhesive to that portion of an IC mounting surface on which said IC is not to be located.

17. (withdrawn) The multi-layer circuit wiring board according to claim 16, which said fixing frame is made of a metal or resin.

18. (withdrawn) A multi-layer circuit wiring board comprising:

a first film having a first wiring pattern formed on one surface thereof, a second wiring pattern formed on another surface thereof, and a first via-contact layer electrically connecting said first wiring pattern with said second wiring pattern;

a second film provided with a third wiring pattern on one surface thereof, another surface thereof being superimposed on said one surface of said first film;

a third film provided with a fourth wiring pattern on one surface thereof, another surface thereof being superimposed on the other surface of said first film;

a second via-contact layer for electrically connecting said first wiring pattern with said third wiring pattern;

a third via-contact layer for electrically connecting said second wiring pattern with said fourth wiring pattern;

a fourth film provided with a fifth wiring pattern for mounting an IC on one surface thereof, another surface thereof being superimposed on said second film;

a fifth film provided on one surface thereof with a sixth wiring pattern to be electrically connected with a printed wiring board, another surface thereof being superimposed on said third film;

a fourth via-contact layer for electrically connecting said third wiring pattern with said fifth wiring pattern; and

a fifth via-contact layer for electrically connecting said fourth wiring pattern with said sixth wiring pattern.

19. (withdrawn) The multi-layer circuit wiring board according to claim 18, wherein said first film comprises a polyimide resin layer and a first and a second wiring patterns each formed of copper and formed on said polyimide resin layer; said second film comprises a polyimide resin layer and a third wiring pattern formed of copper and formed on said polyimide resin layer; said third film comprises a polyimide resin layer and a fourth wiring pattern formed of copper and formed on said polyimide resin layer; said fourth film comprises a polyimide resin layer and a fifth wiring pattern formed of copper and formed on said polyimide resin layer; and

said fifth film comprises a polyimide resin layer and a sixth wiring pattern formed of copper and formed on said polyimide resin layer.

20. (withdrawn) The multi-layer circuit wiring board according to claim 18, which further comprises:

a first adhesive layer for bonding said second film to said first film;

a second adhesive layer for bonding said third film to said first film;

a third adhesive layer for bonding said fourth film to said second film; and

a fourth adhesive layer for bonding said fifth film to said third film.

21. (currently amended) A multi-layer circuit wiring board comprising a laminate of resin films and an adhesive layer for bonding said films, each resin film having a wiring pattern formed on at least one surface thereof, wherein the wiring pattern formed on one resin film is electrically connected with a wiring pattern formed on another resin film which is disposed next to said one resin film, through a via-contact layer provided on said one resin film or on said another resin film, a wiring pattern formed on an outermost resin film on one side of said laminate is a wiring pattern for mounting an IC, and a wiring pattern formed on another outermost resin film on another side of said laminate is a wiring pattern to be electrically connected with a printed wiring board, each of said films having a thickness of 12.5 μm to 80 μm, and said adhesive layer having a thickness of 30 μm or less.

22. (withdrawn) An IC package comprising an IC, and a multi-layer circuit wiring board mounting said IC, wherein said multi-layer circuit wiring board comprising:

a first film having a first wiring pattern formed on one surface thereof, a second wiring pattern formed on another surface thereof, and a first via-contact layer electrically connecting said first wiring pattern with said second wiring pattern;

a second film provided with a third wiring pattern for mounting an IC on one surface thereof, another surface thereof being superimposed on said one surface of said first film;

a third film provided on one surface thereof with a fourth wiring pattern to be electrically connected with a printed wiring board, another surface thereof being superimposed on said other surface of said first film;

a second via-contact layer for electrically connecting said first wiring pattern with said third wiring pattern; and

a third via-contact layer for electrically connecting said second wiring pattern with said fourth wiring pattern.

23. (withdrawn) The IC package according to claim 22, wherein said first film comprises a polyimide resin layer and a first and a second wiring patterns each formed of copper and formed on said polyimide resin layer; said second film comprises a polyimide resin layer and a third wiring pattern formed of copper and formed on said polyimide resin layer; and said third film comprises a polyimide resin layer and a fourth wiring pattern formed of copper and formed on said polyimide resin layer.

24. (currently amended) An IC package comprising an IC, a multi-layer circuit wiring board mounting said IC, and a printed wiring board mounting said multi-layer circuit wiring board, wherein said multi-layer circuit wiring board comprising:

a first film having a first wiring pattern formed on one surface thereof, a second wiring pattern formed on another surface thereof, and a first via-contact layer electrically connecting said first wiring pattern with said second wiring pattern;

a second film provided with a third wiring pattern for mounting an IC on one surface thereof, another surface thereof being superimposed on said one surface of said first film;

a third film provided on one surface thereof with a fourth wiring pattern to be electrically connected with a printed wiring board, another surface thereof being superimposed on the other surface of said first film;

a second via-contact layer for electrically connecting said first wiring pattern with said third wiring pattern; ~~and~~

a third via-contact layer for electrically connecting said second wiring pattern with said fourth wiring pattern;

a first adhesive layer for bonding said second film to said first film; and

a second adhesive layer for bonding said third film to said first film, each of said first, second and third films having a thickness of 12.5 μm to 80 μm, and each of said adhesive layers having a thickness of 30 μm or less.

25. (withdrawn) The IC package according to claim 22, wherein said first film comprises a polyimide resin layer and a first and a second wiring patterns each formed of copper and formed on said polyimide resin layer; said second film comprises a polyimide resin

layer and a third wiring pattern formed of copper and formed on said polyimide resin layer; and said third film comprises a polyimide resin layer and a fourth wiring pattern formed of copper and formed on said polyimide resin layer.

26. (withdrawn) The IC package according to claim 22, which further comprises a first adhesive layer for bonding said second film to said first film, and a second adhesive layer for bonding said third film to said first film.

27. (withdrawn) The IC package according to claim 26, wherein each of said adhesive layers is formed of a thermosetting adhesive layer containing an epoxy curing component.

28. (withdrawn) The IC package according to claim 26, wherein the thickness of each of said adhesive layers is 30 μm or less.

29. (withdrawn) The IC package according to claim 22, wherein said first via-contact layer, said second via-contact layer and said third via-contact layer are all formed of a blind via-contact layer, and the ratio of the diameter of the bottom of each of these via-contact layer to the diameter of the top opening of each of these via-contact layer is within the range of 0.2 to 1.0.

30. (withdrawn) The IC package according to claim 22, wherein said first via-contact layer, said second via-contact layer and said third via-contact layer are all formed of a blind via-contact layer, and the ratio of the diameter of the bottom of each of these via-contact layers to the diameter of the top opening of each of these via-contact layers is within the range of 0.4 to 0.8.

31. (withdrawn) The IC package according to claim 22, wherein said IC is electrically connected with said multi-layer circuit wiring board by way of face-down bonding.

32. (withdrawn) The IC package according to claim 22, wherein said IC is electrically connected with said multi-layer circuit wiring board by way of wire bonding using a gold or aluminum wire.

33. (withdrawn) The IC package according to claim 22, wherein said IC is sealed with a resin.

34. (withdrawn) The IC package according to claim 31, wherein said IC is laminated with a metal plate and then sealed.

35. (cancelled)

36. (cancelled)

37. (cancelled)

38. (cancelled)

38. (cancelled)

40. (cancelled)

41. (cancelled)

42. (cancelled)

43. (cancelled)

44. (cancelled)

44. (cancelled)

45. (cancelled)

47. (cancelled)

48. (cancelled)

49. (cancelled)

50. (cancelled)

51. (cancelled)

52. (new) The multi-layer circuit wiring board according to claim 1, wherein said wiring pattern has a tapered side surface.

53. (new) The multi-layer circuit wiring board according to claim 21, wherein said wiring pattern has a tapered side surface.

54. (new) The multi-layer circuit wiring board according to claim 24, wherein said wiring pattern has a tapered side surface.